# *Extracting low-precision floating-point adders from embedded hard FP DSP Blocks on FPGAs*

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Intel Corporation

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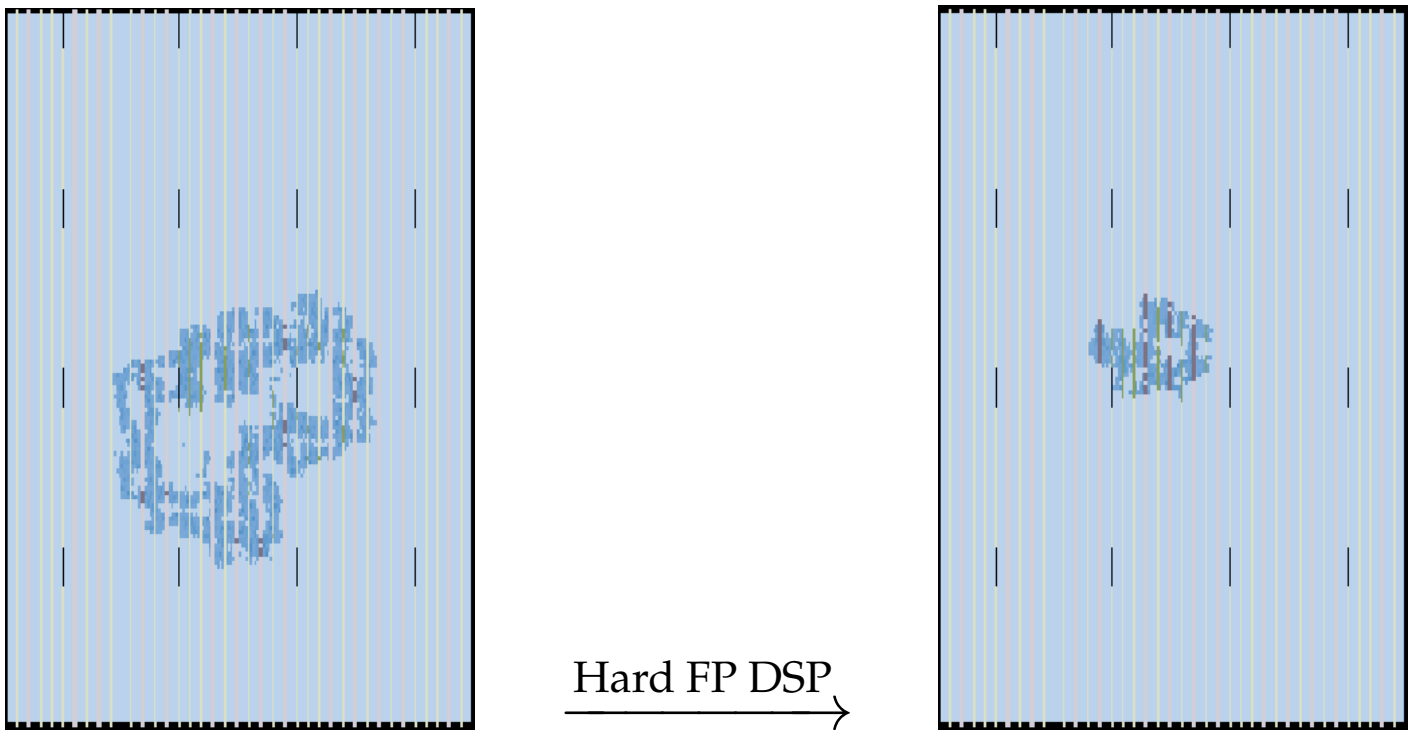
# Context

Contemporary FPGAs embed DSP Blocks with new FP functionality



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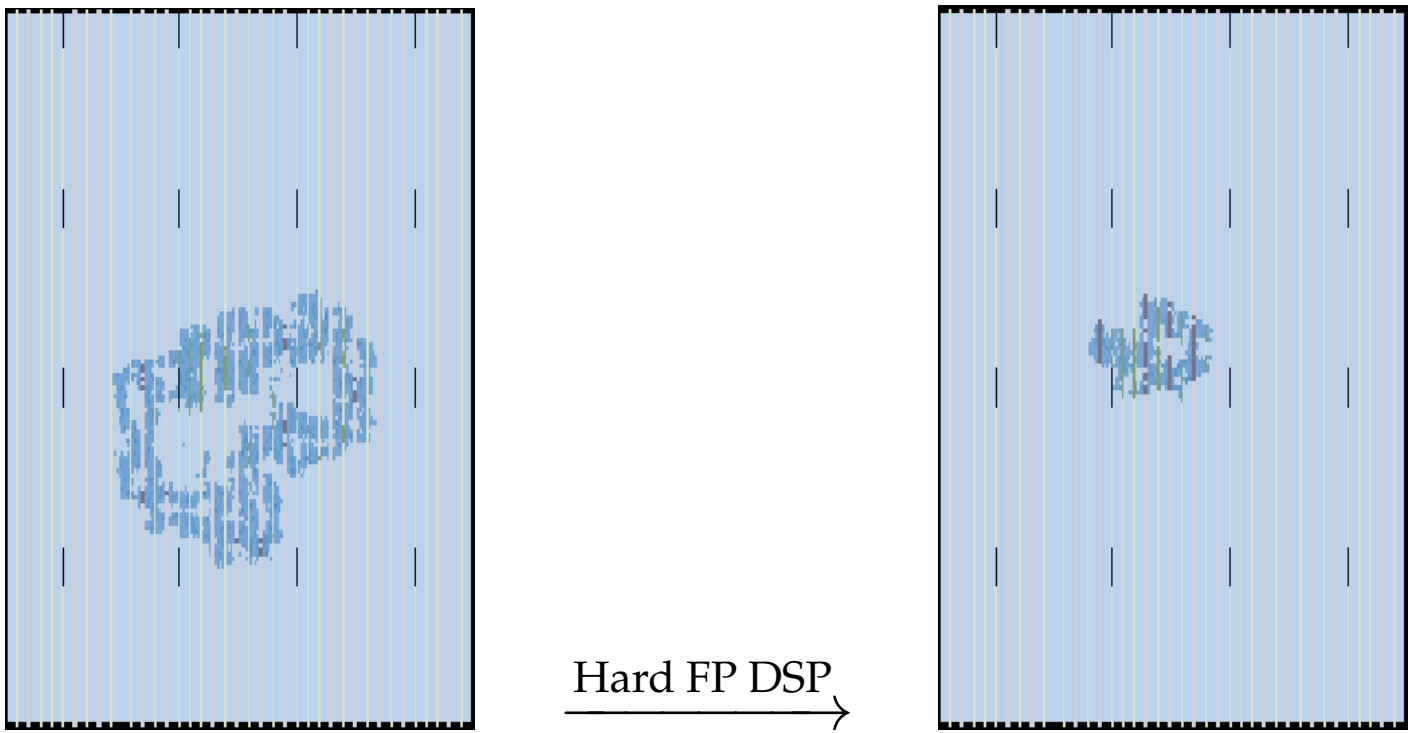
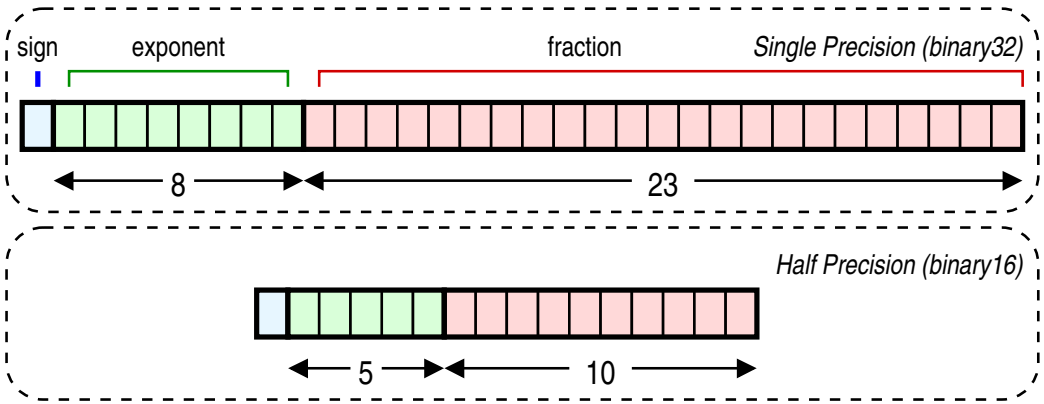



How to use this functionality for low-precision FP adders?

# Background

## IEEE-754 formats single (32-bit) and half (16-bit) precision

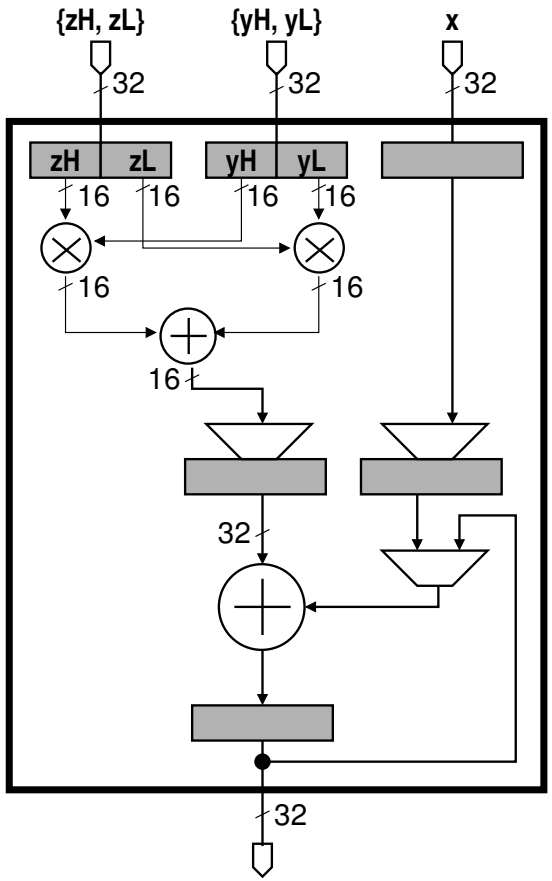



## Exception Encoding

| Encoded Value | Exponent | Fraction |
|---|---|---|
| Zero (flush mode) | 0 | Any |
| Zero (subnormals) | 0 | 0 |
| Subnormal | 0 | $\neq 0$ |
| Regular | 00..01 $\rightarrow$ 11..10 | Any |
| Infinity | 11..11 | 0 |
| NaN | 11..11 | $\neq 0$ |

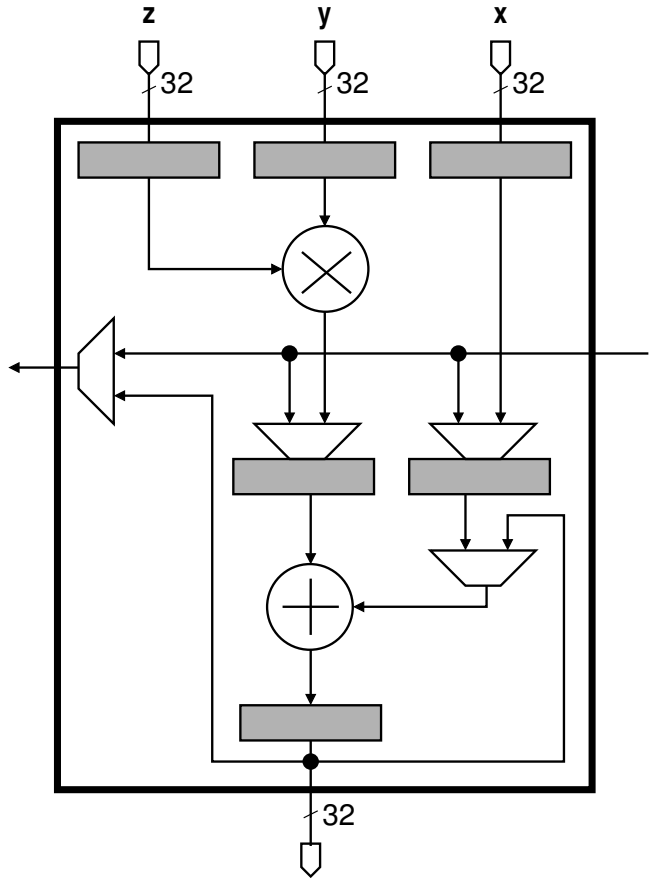
# Background

Agilex DSP Block
in low-precision FP mode




$$D = (yH \cdot zH + yL \cdot zL) + x$$

SP DSP Block
Agilex, Stratix 10, Arria 10

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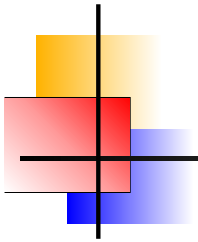

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$D = (yH \cdot zH + yL \cdot zL) + x$

$yY$, $yL$, $zH$ and $zL$ are all HP values,
$x$ and $D$ are in SP.

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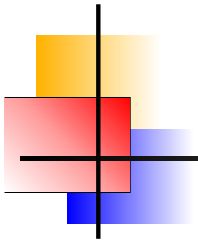
- Subtlety that $x = -0$ allows maintaining the correct sign for 0.



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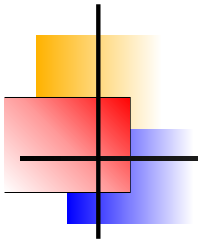

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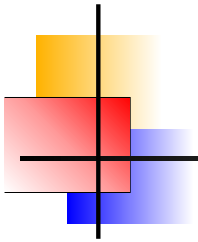

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$$\begin{aligned} e_S^b &= (e_D^b - 127) + 15 \\ &= e_D^b - 112. \end{aligned}$$

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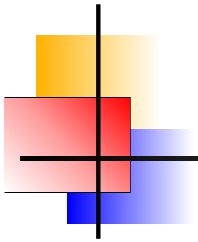

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Check the effect of exponent subtraction on exception case encodings:
For **Infinity** and **NaN** $e_D^b = 255$:

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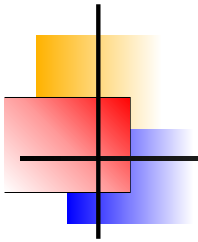

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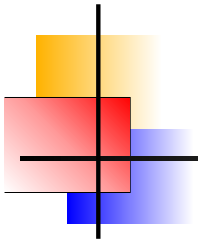

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Lower 4-bits match desired encoding, bit 5 needs inverting.

# HP FP Add Architecture - Agilex

| $e_D^b$ | $e_D^u$ | Binary | Class | $e_D^b$-112 | Binary | Goal |
|---|---|---|---|---|---|---|
| 255 | - | 1111 1111 | Inf/NaN | 143 | 1 000 1111 | 1 1111 |
| 142 | 15 | 1000 1110 | Regular | 30 | 0 001 1110 | 1 1110 |
| 141 | 14 | 1000 1101 | Regular | 29 | 0 001 1101 | 1 1101 |
| ... | | | | | | |
| 128 | 1 | 1000 0000 | Regular | 16 | 0 001 0000 | 1 0000 |
| 127 | 0 | 0111 1111 | Regular | 15 | 0 000 1111 | 0 1111 |
| 126 | -1 | 0111 1110 | Regular | 14 | 0 000 1110 | 0 1110 |
| ... | | | | | | |
| 114 | -13 | 0111 0010 | Regular | 2 | 0 000 0010 | 0 0010 |
| 113 | -14 | 0111 0001 | Regular | 1 | 0 000 0001 | 0 0001 |
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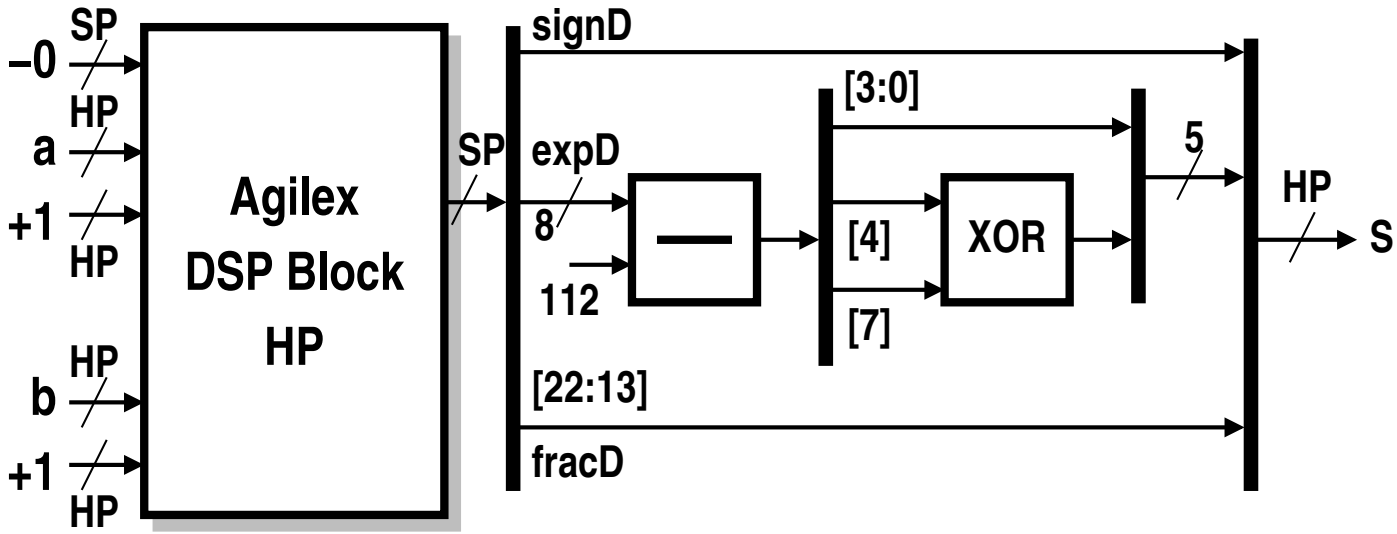
Correctly rounded HP implementation based on the Agilex DSP Block



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| 255 | - | 1111 1111 | Inf/NaN | 143 | 1000 1111 | 11111 |
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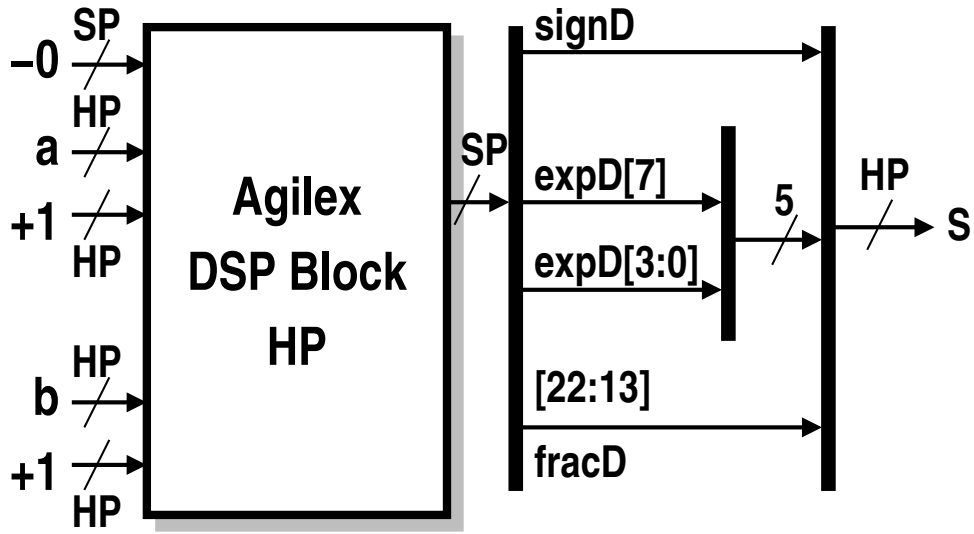

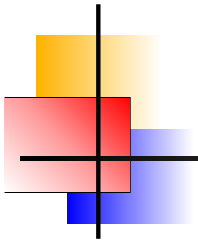

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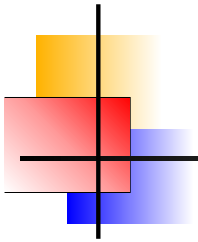
- Use SP DSP Block present in Arria 10, Stratix 10 or Agilex
- First step: HP $\xrightarrow{convert}$ SP
  - fraction: right padding with 13 zeros
  - exponent: 5-bit $\rightarrow$ 8-bit can be done via table lookup



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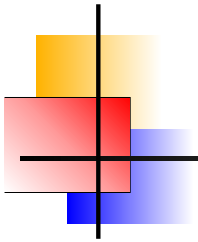
- Use custom conversion, $x_{\mathrm{HP}} \neq x_{\mathrm{SP}}$
- Benefit from exception handling of SP FP Adder



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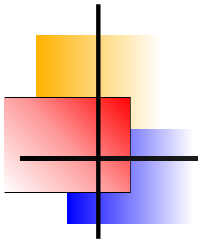
Reliably recover output Inf and NaN conditions



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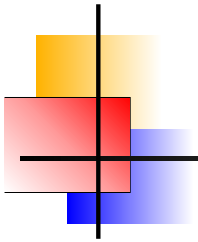

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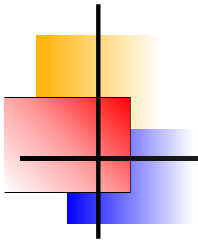
Why does this work? What about double-rounding?

- If no SP rounding occurs $\rightarrow$ easy to prove
- SP rounding has occurred when exponent difference $\geq 14$
- HP fraction is only 10 bits wide
- Rounded result far from HP midpoint.



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- tabulation would require 8-bit table inputs $\rightarrow$ inefficient
- minimum 8-bit exponent 224-10=214 (smallest subnormal).
- observe binary exponent pattern

| Exponent Value | Binary Encoding |
|---|---|
| 255 | 1111 1111 |
| ... | 111x xxxx |
| 224 | 1110 0000 |
| 223 | 1101 1111 |
| ... | 1101 xxxx |
| 215 | 1101 0111 |
| 214 | 1101 0110 (smallest denormal, half) |
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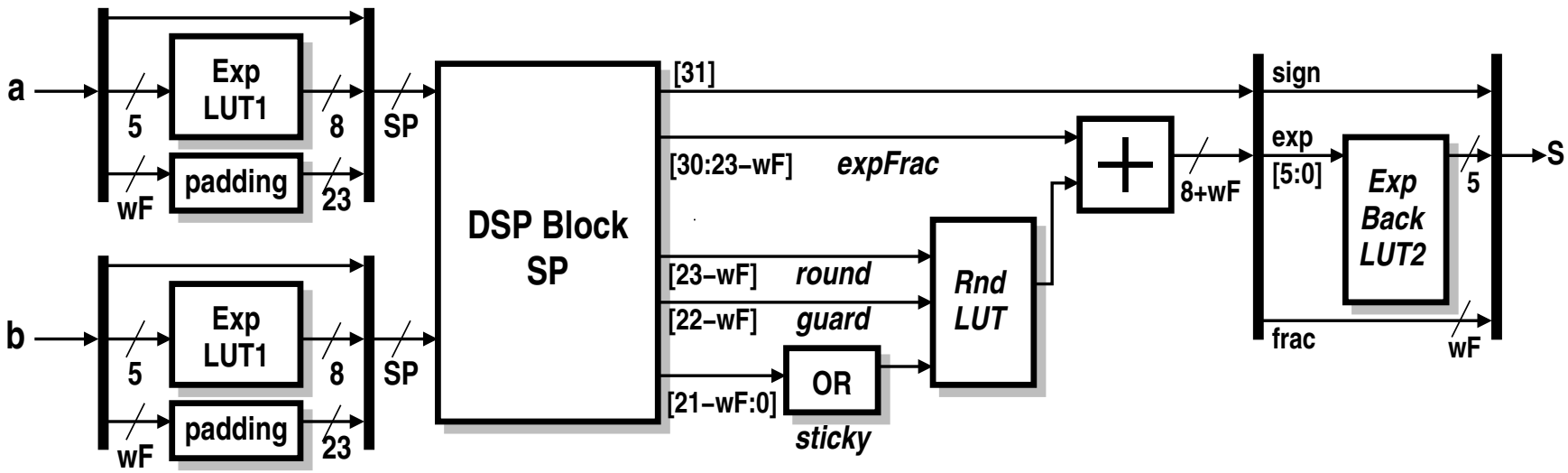
Reverse exponent mapping can be performed with only 6 bits

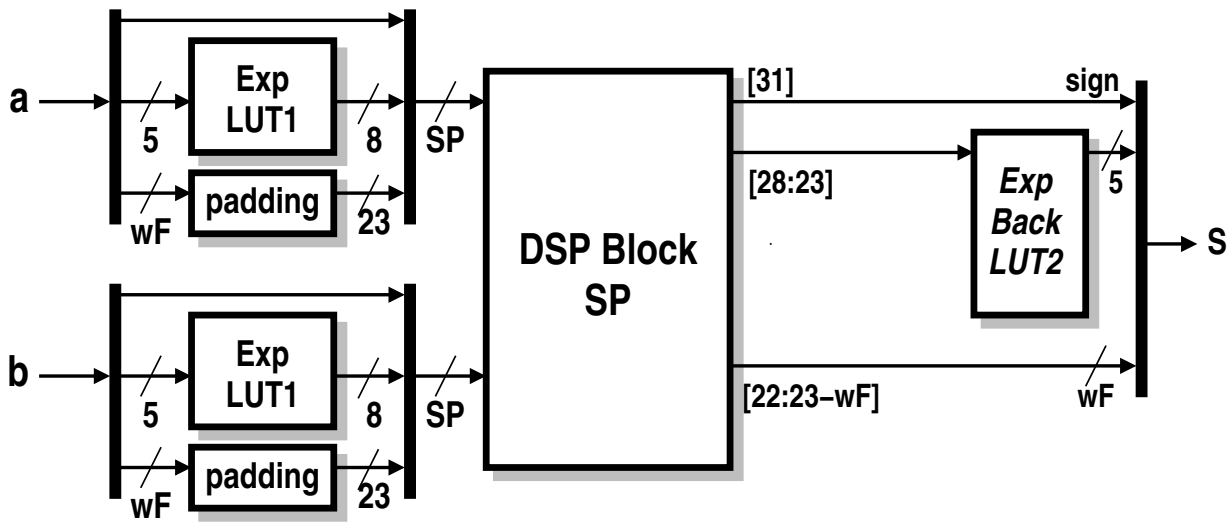
# HP FP Add Architecture - SP DSP Block Mapping

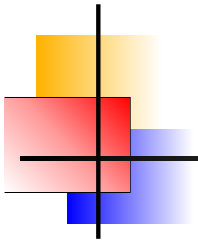
Correctly rounded HP implementation using the SP Hard DSP Block



# HP FP Add Using SP DSP Blocks - Faithful rounding

- faithful rounding can be obtained by means of truncation.
- fraction is directly truncated to 10 bits.

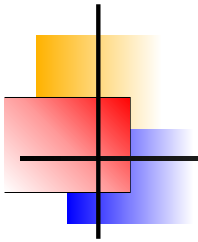




# Results

- logic implementation → Quartus 22.4 fp_functions Megacore.
- generated for a target frequency of 500 MHz.
- synthesis on the fastest speedgrades.

| Arch | Target | Latency | ALMs | DSPs | Ratio |
|---|---|---|---|---|---|
| Proposed-A1 | Agilex | 5 | 5 | 1 | 147 |
| Proposed-A2 | Agilex | 5 | 0 | 1 | 152 |
| Logic | 500MHz, -1 | 11 | 152 | 0 | - |
| Proposed-B | Statix10 | 6 | 26 | 1 | 174 |
| Logic | 500MHz, -1 | 16 | 200 | 0 | - |

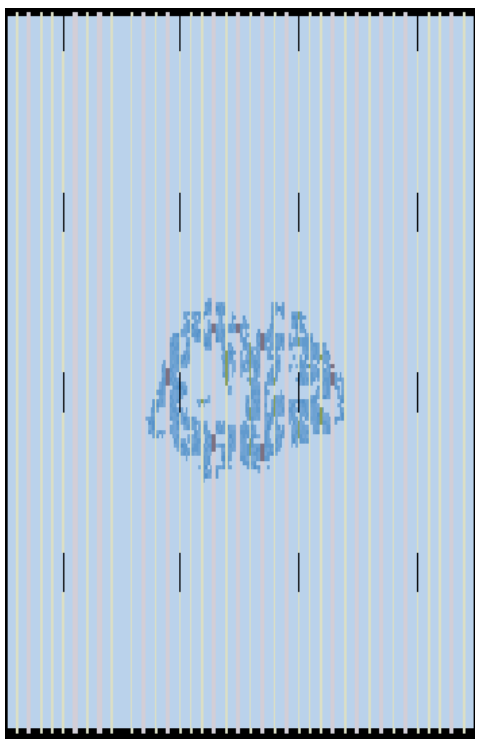


# System Level Impact

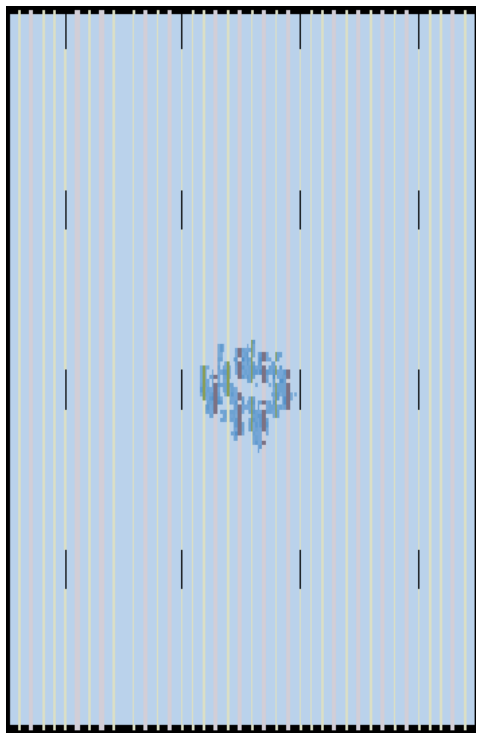
- 8K-point FP FFT design from DSP Builder Advanced
- push-button resource tradeoff using new adder architectures
- target is an Agilex FPGA
- resource utilization: 64 ALMs reduction, 32 DSPs increase
- ratio: 185 ALMs / DSP

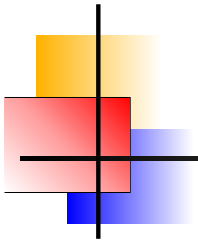
| Architecture | ALMs | M20K | DSPs |
|---|---|---|---|
| Old | 8116 | 62 | 12 |
| Proposed | 2183 | 46 | 44 |

# System Level Impact - Chip-Planner View



Proposed Architectures





# Conclusion

- FPGA DSP Blocks can support HP FP adder architectures.
- Bounding exponent values can help reduce resources.
- Bit-pattern representations exploits can also improve resources.
- System-level improvements may exceed local savings.
- Reduced routing improves system performance.
- Alternative architecture always useful.