AI-based Timing Error Modelling: A Case Study on a Pipelined Floating-point Core

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The adoption of aggressively down-scaled voltages along with worsening process variations render nanometer devices prone to timing errors that threaten system functionality [1, 2]. Recent studies tried to predict timing errors using machine learning (ML), while considering some workload characteristics [3, 4, 5]. However, successfully training such models is challenging, since traditionally acquired samples are insufficient, especially in operating regions where timing errors occur rarely.

In this study, we develop a cross-layer framework, depicted in Figure 1, which utilizes Artificial Intelligence (AI) algorithms and circuit-level simulation to accurately predict timing errors in pipelined cores. Our framework utilizes stochastic search-based techniques to generate microarchitecture-aware samples in various operating regions. To achieve this, we combine post-layout dynamic timing analysis and genetic algorithms, considering the data-dependent path sensitization and instruction execution history. The generated samples are utilized for training accurate error prediction models based on machine-learning (ML) algorithms.

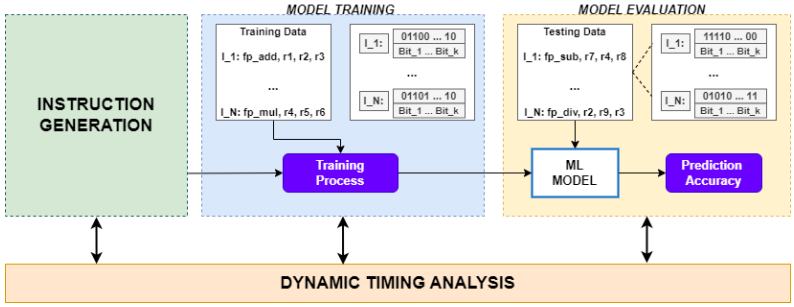

Figure 1: Proposed Framework

We apply our approach to a pipelined IEEE-754 compatible floating-point unit. The evaluation is completed for various applications under different operating settings, showing over 99.8% prediction accuracy, combined with up to a 115.2% increase of the true positive rate in real test data compared to prior error prediction models.

References

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